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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/807,067	04/06/2001	Walter Jan August De Coster	PHQ99.010	2192

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EXAMINER
GUERRERO, MARIA F

ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 12/17/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/807,067	DE COSTER ET AL.	
	Examiner	Art Unit	
	Maria Guerrero	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 October 2002* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. This Office Action is in response to the Amendment filed October 3, 2002.

Claims 1-9 are pending.

Priority

2. This Application is a 371 of PCT/EP00/07519 filed August 2, 2000.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-4, 6-8 are rejected under 35 U.S.C. 102(b) as being anticipated by Kawaguchi (U.S. 5,739,573) (cited by Applicant).

Kawaguchi teaches forming spacers at the sides of a projecting polysilicon region, the spacers having a smaller isolation layer in contact with the projecting polysilicon region, and a larger isolation layer (Fig. 5B-5B, col. 10, lines 10-33). Kawaguchi discloses anisotropically etching at least the vertical portion of the smaller isolation layer to form a trench, the trench being between the larger isolation layer and the corresponding side of the projecting polysilicon region, and the depth of trench being equal to maximally half the height of the larger isolation layer and maximally half the thickness of the larger isolation layer (Fig. 5C, col. 10, lines 35-50). Kawaguchi teaches subjecting the projecting polysilicon region to a silicidation process by

directional depositing a metal layer capable of forming a metal silicide (Fig. 5D-5E, col. 10, lines 65-67, col. 11, lines 1-30).

Kawaguchi teaches an integrated circuit comprising lateral isolation regions formed at the sides of at least one projecting region of polysilicon (Fig. 5B, 7B). Kawaguchi shows each lateral region being composed of a smaller isolation layer and a larger isolation layer, each lateral isolation region comprising a vertical trench made in the smaller isolation layer (Fig. 5C, 7C). Kawaguchi teaches the integrated circuit comprising a metal silicide situated in the upper part of the polysilicon region (Fig. 5E, 7E).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1, 5-6, and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lur et al. (U.S. 6,013,569) in view of Kawaguchi (U.S. 5,739,573).

Lur et al. teaches forming spacers at the sides of a projecting polysilicon region, the spacers having a smaller isolation layer in contact with the projecting polysilicon region, and a larger isolation layer (Fig. 7-8, col. 8, lines 10-35). Lur et al. discloses isotropically etching at least the vertical portion of the smaller isolation layer to form a trench, the trench being between the larger isolation layer and the corresponding side of the projecting polysilicon region (Fig. 8, col. 8, lines 45-65). Lur et al. teaches subjecting

the projecting polysilicon region to a silicidation process by directional depositing a metal layer capable of forming a metal silicide (Fig. 9, col. 9, lines 3-15, 35-45).

In addition, Lur et al. teaches an integrated circuit comprising lateral isolation regions formed at the sides of at least one projecting region of polysilicon, each lateral region being composed of a smaller isolation layer and a lager isolation layer. Lur et al. shows each lateral isolation region comprising a vertical trench made in the smaller isolation layer, a horizontal trench made in the smaller isolation layer between the larger isolation layer and the substrate (Fig. 8). Lur et al. teaches the integrated circuit comprising a metal silicide situated in the upper part of the polysilicon region (Fig. 9).

Lur et al. forming the smaller isolation layer by depositing over and around the plolysilicon in a single step. However, Kawaguchi teaches forming the smaller isolation layer by depositing over and around the plolysilicon in a single step (Fig. 5A, 9A, col. 10, lines 18-20).

Therefore, It would have been obvious to a person of ordinary skill in the art at the time of the invention to modify Lur et al. reference by including the teaching of Kawaguchi because chemical vapor deposition is conventional use in the art to depositing insulating films. The modification is proper because the chemical vapor deposition would avoid unnecessary oxidation of the polysilicon film.

Response to Arguments

5. Applicant's arguments filed October 3, 2002 have been fully considered but they are not persuasive. Claims1-4 and 6-8 stand rejected.

Applicant argued that Kawaguchi fails to describe the depth of trench being equal to maximally half the height of the larger isolation layer. However, Kawaguchi shows the depth of trench being equal to maximally half the height of the larger isolation (Fig. 5C, col. 10, lines 35-50).

Applicant's arguments with respect to claims 5 and 9 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

6. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Maria Guerrero whose telephone number is 703-305-0162.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on 703-308-4905. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

MG
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December 11, 2002

AMIR ZARABIAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800